IN THE CLAIMS

What is claimed is:

1-5. (Cancelled)

6. (Currently Amended) The bus bridge of Claim ~~4~~ 18, wherein the first serial bus interface is an ~~IIC~~ Inter-Integrated Circuit (IIC) bus interface.

7-8. (cancelled)

9. (Currently amended) A bus bridge comprising:

a first serial bus interface, the first serial bus interface operable as a bus slave;

apparatus for selecting a particular target serial bus port of a plurality of target serial bus ports, the apparatus for selecting a particular target bus port addressable through the first bus interface, wherein the plurality of target ports comprises at least two JTAG bus ports;

~~apparatus for coupling to the particular target bus port, the apparatus for coupling operable as a bus master~~;

apparatus for transferring information between the first serial bus interface and the particular target serial bus port, the apparatus for transferring information operable as a bus master on the particular bus port.

10. (Cancelled)

11. (Currently Amended) The bus bridge of Claim ~~10~~9, wherein the first serial bus interface is an IIC bus interface.

12. (Currently Amended) The bus bridge of Claim 11, wherein the apparatus for transferring information between the first bus interface and the particular target serial bus port ~~coupling the first bus interface to the apparatus for coupling to a plurality of target serial~~ bus ports comprises at least one FIFO.

13. (Currently Amended) The bus bridge of Claim 12, further comprising a bypass mechanism whereby data may be communicated between the first serial bus interface and ~~apparatus for coupling to a plurality of~~ the particular target serial ~~busses~~ bus without using the ~~FIFOS~~ at least one FIFO.

14. (Currently Amended) The bus bridge of Claim 13, implemented in an ~~FPGA~~ Field Programmable Gate Array (FPGA) having an associated EEPROM for storing configuration code.

15. (Currently Amended) The bus bridge of Claim 14, wherein a serial bus port of the target serial ~~busses~~ bus ports is coupled to the EEPROM, and wherein the EEPROM may be erased and written through the serial bus.

16. (Currently Amended) The bus bridge of Claim 15, wherein the serial bus port of the target serial busses that is coupled to the EEPROM is also coupled to a configuration header.

17. (Currently Amended) The bus bridge of Claim 11, implemented in a bus bridge FPGA having an EEPROM associated therewith for storing configuration code, wherein a selected serial bus port of the target serial bus ports is coupled to the EEPROM associated with the bus bridge FPGA, and wherein the EEPROM associated with the bus bridge FPGA may be erased and written through the selected target serial bus port, thereby permitting modification of the bus bridge.

18. (New) A bus bridge comprising:

a first serial bus interface, the first serial bus interface operable as a bus slave;

a target serial bus interface comprising a plurality of target serial bus ports;

selection logic coupled such that the first serial bus interface can designate a selected target serial bus port of the plurality of target serial bus ports, and wherein the target serial bus interface is operable as a bus master on the selected target serial bus port; and

apparatus coupling the first serial bus interface to the target serial bus interface, such that commands received by the first bus interface are capable of causing execution of commands by the target serial bus interface on the selected target serial bus port, the apparatus coupling the first serial bus interface to the target serial bus interface further comprising at least one First-In-First-Out (FIFO) buffer and a status register having flags for detecting data in the at least one FIFO buffer;

wherein the target serial bus interface is a Joint Test Action Group (JTAG) bus interface.

19. (New) The bus bridge of claim 18, implemented in a bus bridge FPGA having an EEPROM associated therewith for storing configuration code, wherein a selected serial bus port of the target serial bus ports is coupled to the EEPROM associated with the bus bridge FPGA, and wherein the EEPROM associated with the bus bridge FPGA may be erased and written through the selected target serial bus port, thereby permitting modification of the bus bridge.

20. (New) The bus bridge of claim 19, wherein the apparatus coupling the first serial bus interface to the target serial bus interface has a bypass mode such that the EEPROM associated with the bus bridge FPGA can be erased and written without using the at least one FIFO buffer.

21. (New) The bus bridge of claim 17, wherein the apparatus for transferring information has a bypass mode such that the EEPROM associated with the bus bridge FPGA can be erased and written without using the at least one FIFO buffer